FIG. 1

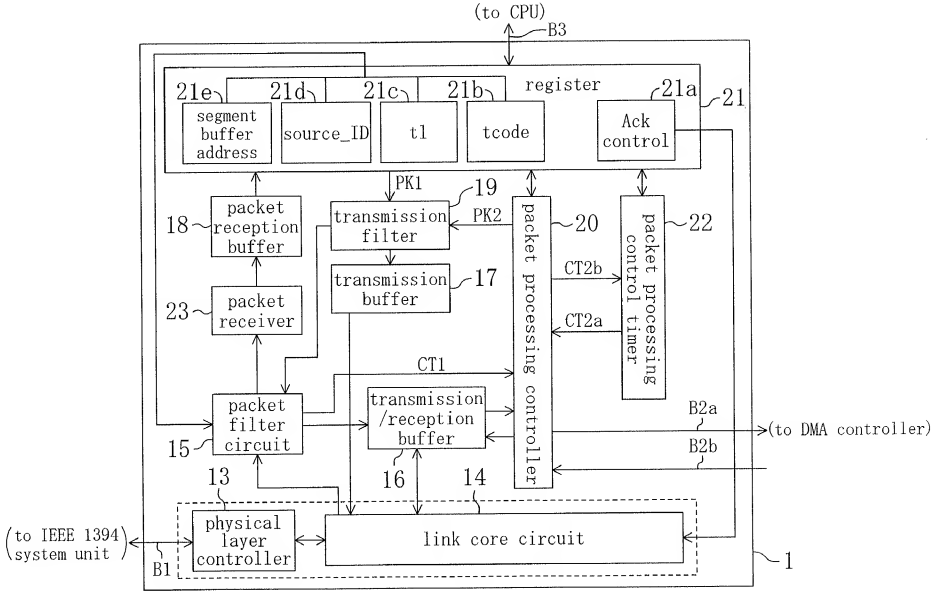
(to CPU)
B3
21e
21d
21c
21b
register
21a
21
segment buffer address
source_ID
tl
tcode
Ack control
PK1
19
18
packet reception buffer
transmission filter
PK2
20
packet processing controller
22
packet processing control timer
transmission buffer
17
CT2b
CT2a
23
packet receiver
CT1
packet filter circuit
transmission /reception buffer
B2a
(to DMA controller)
B2b
15
13
16
14
(to IEEE 1394 system unit)
physical layer controller
link core circuit
B1
1

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FIG. 2

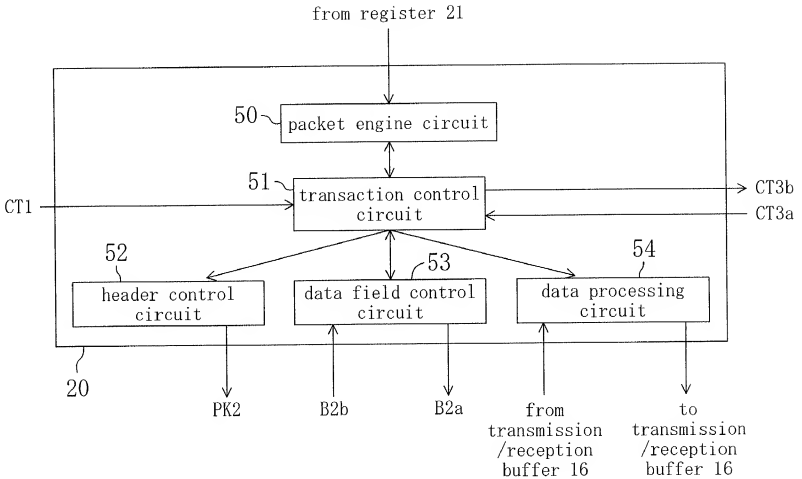

FIG. 3

Block write request transmit format

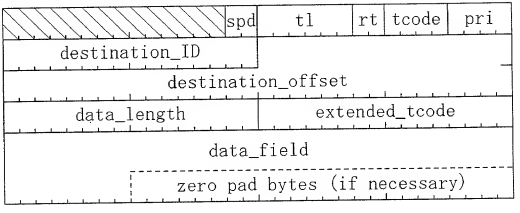

FIG. 4

Quadlet write request transmit format

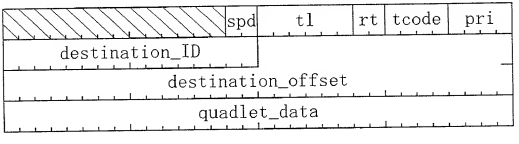

FIG. 5

Write response receive format

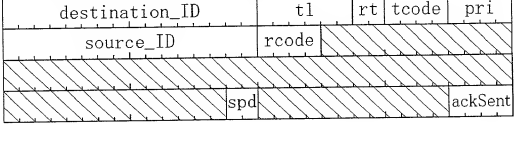

FIG. 6

Block read request transmit format

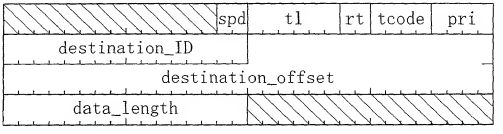

FIG. 7

Block read response receive format

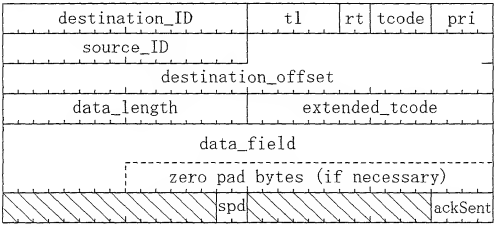

FIG. 8

Write request for data block packet format

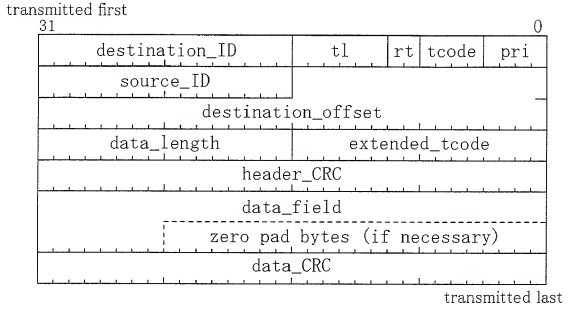

FIG. 9

Write request for data quadlet packet format

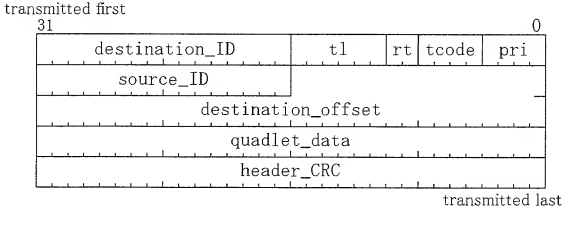

FIG. 10

Write response packet format

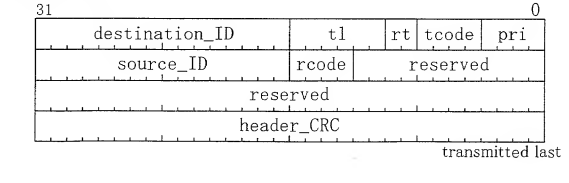

FIG. 11

Read request for data block packet format

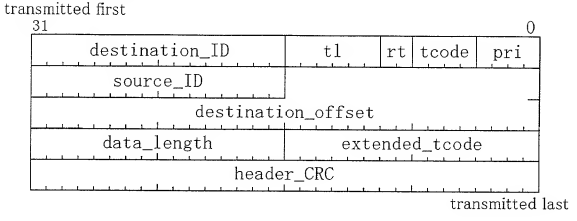

FIG. 12

Read response for data block packet format

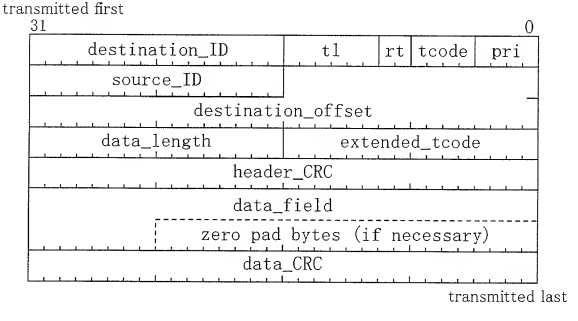

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FIG. 13

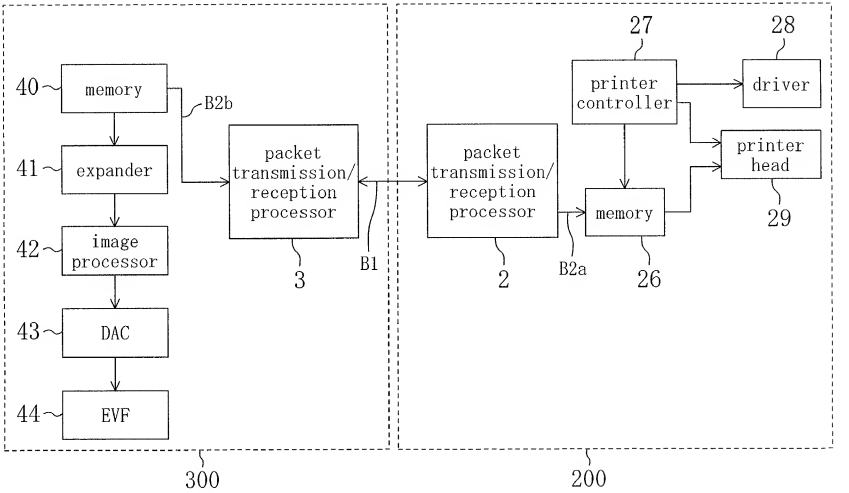


FIG. 14

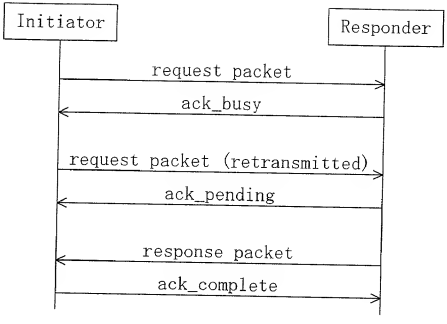

Initiator
Responder
request packet
ack_busy
request packet (retransmitted)
ack_pending
response packet
ack_complete

FIG. 15

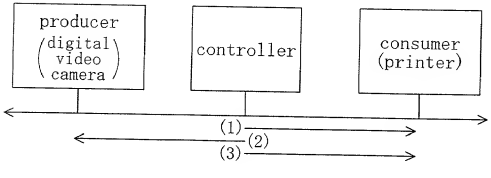

producer
(digital video camera)
controller
consumer
(printer)
(1)
(2)
(3)

FIG. 16

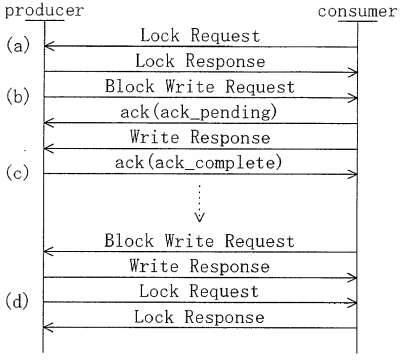
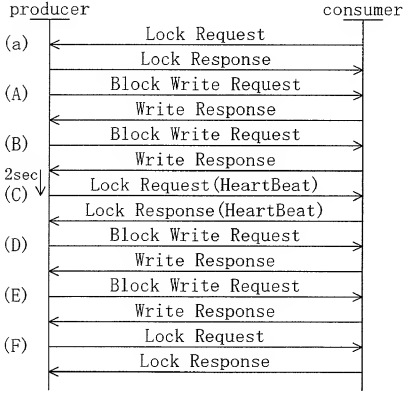

producer
consumer
(a)
Lock Request
Lock Response
(b)
Block Write Request
ack(ack_pending)
Write Response
(c)
ack(ack_complete)
Block Write Request
Write Response
(d)
Lock Request
Lock Response

FIG. 17


producer
consumer
(a)
Lock Request
Lock Response
(A)
Block Write Request
Write Response
(B)
Block Write Request
Write Response
2sec
(C)
Lock Request(HeartBeat)
Lock Response(HeartBeat)
(D)
Block Write Request
Write Response
(E)
Block Write Request
Write Response
(F)
Lock Request
Lock Response

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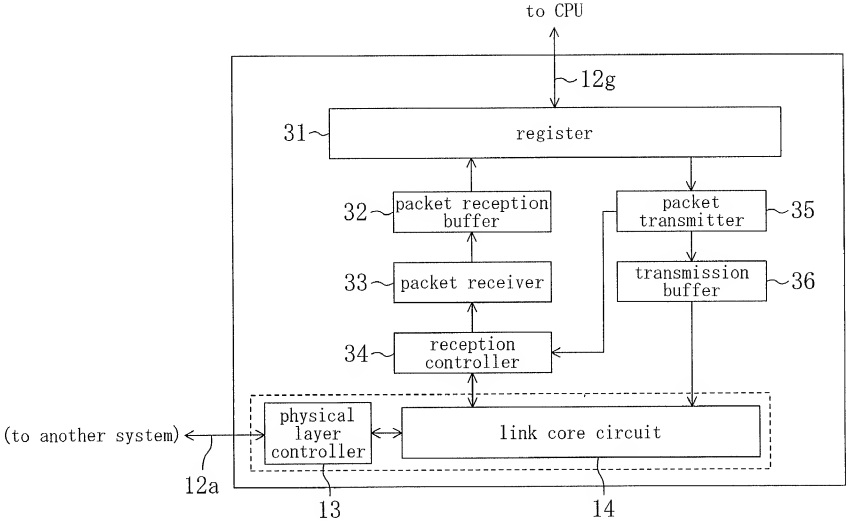
FIG. 18